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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/981,135	10/16/2001	Jeroen Anton Johan Leijten	NL 000576	6206

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EXAMINER	
MEONSKE, TONIA L	
ART UNIT	**PAPER NUMBER**
2183	

DATE MAILED: 08/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/981,135	LEIJTEN ET AL.	
	Examiner	Art Unit	
	Tonia L. Meonske	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 June 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5 and 7-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5, 7-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-5 and 7-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fisher et al., US Patent 6,026,479, cited on the Information Disclosure Statement filed November 17, 2003, in view of Dowling, US Patent 6,128,728 and in view of Trimberger et al., US Patent 5,844,422.

3. Referring to claim 1, Fisher et al. have taught the digital signal processing apparatus comprising a plurality of available hardware resource means and a first instruction set means having access to said available hardware resource means, so that at least a part of said hardware resource means execute operations under control of said first instruction set means (abstract, high ILP, column 7, lines 14-36); the digital signal processing apparatus further comprising a second instruction set means having access to only a predetermined limited subset of said plurality of available hardware resource means, so that at least a part of said predetermined limited subset of said hardware resource means execute operations under control of said second instruction set means (abstract, low ILP, column 7, lines 14-36), wherein in case of an interrupt the state of all hardware resources means under control of said first instruction set means have their state frozen (abstract, The main instruction and data caches are deactivated, or frozen, to preserve their contents.); and wherein at least a part of such hardware resource means which are not directly

accessible and not included in said predetermined limited subset of said hardware resource means are chained together in a first scan chain means (Figure 2, element 120 to element 130 to elements 150A-C to element 180 are chained together in a first scan chain means.) and at least a part of such hardware resources which are not directly accessable and included in said predetermined limited subset of said hardware resource means are chained together in a second scan chain means (Figure 2, element 122 to element 132 to element 150D to element 180 are chained together in a second scan chain means.).

4. Fisher et al. have not taught all of said limited subset of hardware resource means are stored within a single clock cycle. However, Dowling has taught all of said limited subset of hardware resource means are stored within a single clock cycle (abstract). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the invention of Fisher et al. store all of said limited subset of hardware resource means within a single clock cycle, as taught by Dowling, for the desirable purpose of largely eliminating delays associated with register saving and restoring (abstract).

5. Fisher et al. have also not storing the hardware resource means using a plurality of flip-flops. However, Trimberger et al. have taught storing hardware resource means using flip-flops (abstract, column 3, lines 19-35, column 4, lines 46-67) for the desirable purpose of protecting the state data during a processor interruption. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the hardware resource means, as taught by Fisher et al., be stored by using a plurality of flip-flops, as taught by Trimberger et al., for the desirable purpose of protecting the state data during a processor interruption (abstract, column 3, lines 19-35, column 4, lines 46-67).

6. Referring to claim 2, Fisher et al. have taught the apparatus according to claim 1, as described above, and wherein said available hardware resource means are processor resource means (abstract, column 7, lines 14-36).

7. Referring to claim 3, Fisher et al. have taught an apparatus according to claim 1, as described above, and comprising first state buffer means for storing the current state of hardware resource means in case of an interrupt, wherein in case of an interrupt said first state buffer means stores the current state of at least a part of such hardware resource means which are not included in said predetermined limited subset of said hardware resource means (column 6, lines 54-65, Figure 2, elements 120, 180, elements 150A-C).

8. Referring to claim 4, Fisher et al. have taught an apparatus according to claim 3, further comprising second state buffer means for storing in case of an interrupt the current state of at least a part of said predetermined limited subset of said hardware resource means, said second state buffer means having a smaller size than that of said first state buffer means (column 6, lines 54-65, Figure 2, elements 122 and 190, element 150D, column 6, lines 7-26).

9. Referring to claim 5, Fisher et al. have taught an apparatus according to claim 4, as described above, and comprising means for supplying power to said second state buffer means, wherein said power supply means essentially supplies power to said second state buffer means only during interrupt handling (column 7, lines 14-65).

10. Referring to claim 7, Fisher et al. have taught an apparatus according to claim 1, wherein said second instruction set means does not allow operations in parallel (Figure 2, abstract, The second instruction set means executing in element 150D does not allow any operations in 150A-C to be executed in parallel.).

11. Referring to claim 8, Fisher et al. have taught a method for processing digital signals in a digital signal processing apparatus comprising a plurality of available hardware resource means wherein at least a part of said hardware resource means execute operations under control of a first instruction set (abstract, high ILP, column 7, lines 14-36); wherein at least a part of a predetermined limited subset of said plurality of available hardware resource means execute operations under control of a second instruction set having access to only said predetermined limited subset of said hardware resource means (abstract, low ILP, column 7, lines 14-36), wherein in case of an interrupt the state of all hardware resources means under control of said first instruction set means have their state frozen (abstract, The main instruction and data caches are deactivated, or frozen, to preserve their contents.); and wherein at least a part of such hardware resource means which are not directly accessible and not included in said predetermined limited subset of said hardware resource means are chained together in a first scan chain means (Figure 2, element 120 to element 130 to elements 150A-C to element 180 are chained together in a first scan chain means.) and at least a part of such hardware resources which are not directly accessable and included in said predetermined limited subset of said hardware resource means are chained together in a second scan chain means (Figure 2, element 122 to element 132 to element 150D to element 180 are chained together in a second scan chain means.).

12. Fisher et al. have not taught all of said limited subset of hardware resource means are stored within a single clock cycle. However, Dowling has taught all of said limited subset of hardware resource means are stored within a single clock cycle (abstract). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the

invention of Fisher et al. store all of said limited subset of hardware resource means within a single clock cycle, as taught by Dowling, for the desirable purpose of largely eliminating delays associated with register saving and restoring (abstract).

13. Fisher et al. have also not storing the hardware resource means using a plurality of flip-flops. However, Trimberger et al. have taught storing hardware resource means using flip-flops (abstract, column 3, lines 19-35, column 4, lines 46-67) for the desirable purpose of protecting the state data during a processor interruption. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the hardware resource means, as taught by Fisher et al., be stored by using a plurality of flip-flops, as taught by Trimberger et al., for the desirable purpose of protecting the state data during a processor interruption (abstract, column 3, lines 19-35, column 4, lines 46-67).

14. Referring to claim 9, Fisher et al. have taught a method according to claim 8, as described above, and wherein in case of an interrupt the current state of hardware resource means are stored in first state buffer means (column 6, lines 54-65, Figure 2, elements 120, 180, elements 150A-C); wherein in case of an interrupt the current state of at least a part of such hardware resource means which are not included in said predetermined limited subset of said hardware resource means are stored in said first state buffer means (column 6, lines 54-65, Figure 2, elements 120, 180, elements 150A-C).

15. Referring to claim 10, Fisher et al. have taught a method according to claim 9, as described above, and wherein in case of an interrupt the current state of at least a part of said predetermined limited subset of said hardware resource means are stored in a second state buffer

means having a smaller size than that of said first state buffer means (column 6, lines 54-65, Figure 2, elements 122 and 190, element 150D, column 6, lines 7-26).

16. Referring to claim 11, Fisher et al. have taught a method according to claim 10, as described above, and wherein power in essentially supplied to said second state buffer means only during interrupt handling (column 7, lines 14-65).

17. Referring to claim 12, Fisher et al. have taught a method according to claim 8, as described above, and wherein said second instruction set does not allow operations in parallel (Figure 2, abstract, The second instruction set means executing in element 150D does not allow any operations in 150A-C to be executed in parallel.).

Response to Arguments

18. Applicant's arguments with respect to claims 1-5 and 7-12 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

19. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

20. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

21. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tonia L. Meonske whose telephone number is (571) 272-4170. The examiner can normally be reached on Monday-Friday, with every other Friday off.

22. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie P. Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

23. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

tlm

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